implant doses were, 4×10^{16} ion/cm^2 and 5×10^{16} ion/cm^2, respectively, at an energy of 2·5 MeV. Refractive index profiles were determined from the mode spectra which were measured using a prism coupler in the dark mode configuration. Analysis of the mode data was performed using the reflectivity method [2].

Fig. 1 shows the refractive index profile of the $^4He^+$ implanated waveguide. The index increases by ~0·34% near the surface region, and decreases by a small amount (~0·12%) at the end of the ion range, producing in this way a small barrier. In general, nuclear damage domination (at the end of the ion range) leads to a decrease of the refractive index, and a combination of damage ionisation and diffusion may lead to either increase (silica glass) [3] or decrease (some multicomponent glasses) [4]. The optical well type waveguide resulting from refractive index enhancement has better mode confinement as there are nontunnelling modes. Thus, the loss due to leaky modes is completely eliminated.

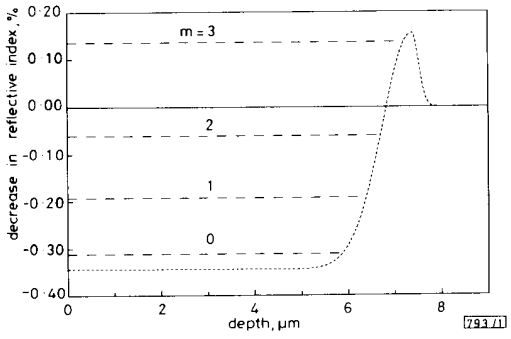

Fig. 1 *Refractive index profile of lead germanate glass after $^4He^+$ at 2·5 MeV and dose of 4×10^{16} ion/cm^2 at 77 K*

Mode values were measured at 633 nm

During ion implantation, ionisation energy may produce colour (absorption) centres which sometimes give high propagation losses within the waveguide. Fortunately, these defects are unstable and they are found to anneal out between 200 and 300°C in this glass.

Loss measurements were performed using the end-coupling configuration. A ×20 microscope objective lens was used to focus an He–Ne (633 nm) laser beam on one polished edge of the sample, and the output light from the waveguide was focused onto a silicon detector connected with a power meter.

Fig. 2 shows the loss reduction with annealing temperature for two waveguides. The first one (solid line) was implanted with $^4He^+$ (2·5 MeV, 4×10^{16} ion/cm^2), and the second one with $^3He^+$ (2·5 MeV, 5×10^{16} ion/cm^2). The $^3He^+$ isotope, because it is lighter, gives a longer range, and thus a wider waveguide and better mode confinement. The loss in the $^3He^+$ implanted guide is lower for most of the annealing temperatures. The spot size of the focused laser beam is ~10 μm, which is larger than the 6·4 μm width of the waveguide, resulting in a launch efficiency of less than 100%. Nevertheless, assuming a 100% launch efficiency the loss, at 200°C for the $^3He^+$ implant, is as low as 0·15 dB/cm. The lowest loss for the $^4He^+$ implanted waveguide is 0·3 dB/cm after the 300°C annealing temperature. For both of the cases we can assume a reproducibility error of ~±0·05 dB/cm. After it reaches its minimum value, for both waveguides, the loss increases due to destruction of the waveguide.

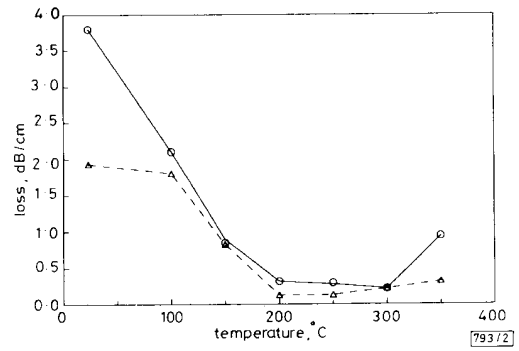

Fig. 2 *Multimode losses for planar waveguides of $^4He^+$ and $^3He^+$ implanted lead germanate glass, after thermal annealing*

○ $^4He^+$
△ $^3He^+$

Conclusions: We have demonstrated the first example of an ion implanted waveguide in lead germanate glass. Furthermore, these guides have the lowest loss ever reported for He ion implanted waveguides in either glass or crystalline substrates. Further optimisation of the edge polishing and minimisation of the surface scattering should lead to even lower propagation losses. This should readily allow lower pumping thresholds and better waveguide laser performance for the rare earth doped lead germanate glass.

26th January 1993

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INTERPOLATOR FILTER STRUCTURE FOR ASYNCHRONOUS TIMING RECOVERY LOOPS

D. Verdin and T. C. Tozer

Indexing terms: Synchronisation, Digital signal processing

A novel structure for the interpolation filter used as a timing-correction element in asynchronous timing recovery loops is introduced. Multirate techniques are employed in an algorithm to institute both bulk and fractional delays in the loop. The performance of the new algorithm is illustrated by generation of the S curves for a two-point NDA tracker and a four-point DD tracker.

Introduction: The generic asynchronous timing-recovery loop is shown in Fig. 1. The input analogue waveform is sampled to give B samples per symbol although the phase of the sam-

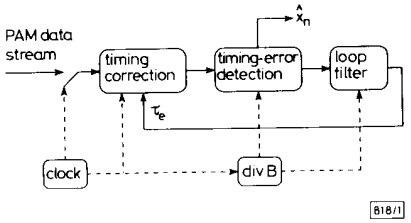

Fig. 1 *Generic model of asynchronous timing-recovery loop*

pling clock may be such that the optimum sampling points are missed. The timing correction block interpolates the correct sampling points according to the fed-back error signal from the error-detection block. The error signal is generated and filtered at the symbol rate.

Examples of timing-error detectors for binary-antipodal filtered data are as follows noting the number of samples per symbol that the scheme requires.

(i) the Meuller and Müller algorithm [1], 1s/s, decision directed:

$$e_t(n) = \hat{x}(n)x(n-1) + x(n)\hat{x}(n-1) \tag{1}$$

(ii) the Gardner algorithm [2], 2s/s, nondata aided:

$$e_t(n) = \{x(n) - x(n-2)\}x(n-1) \tag{2}$$

(iii) four point algorithm [3], 4s/s, decision directed:

$$e_t(n) = \{x(n-1) - x(n-3)\}\hat{x}(n-2) + \alpha\{x(n) - x(n-4)\}\hat{x}(n-2) \tag{3}$$

where $0 \leq \alpha \leq 1$.

In the above the $x(.)$ represent the sampled PAM data stream and the $\hat{x}(.)$ represent receiver decisions.

For timing recovery, the function of the timing-correction block is to institute a delay of up to B samples.

Fractional delay using multirate polyphase filter: It is well known that we can achieve fractional delays by using multirate techniques [4]. The x_n samples out of the ADC are upsampled by a factor U and then filtered by an image-rejection or interpolation filter to produce $B \times U$ sample points per symbol. This sequence can then be delayed to choose those points closer to the optimum sampling points and then downsampled by a factor U. If M is the number of taps in the interpolation filter and we arrange it such that $M = U \times K$ then the process of upsampling and interpolation by a factor U can be represented as

$$\begin{bmatrix} y_n \\ y_{n-1} \\ \vdots \\ y_{n-U} \end{bmatrix} = \begin{bmatrix} h_0 & h_U & \cdots & h_{(K-1)U} \\ h_1 & h_{U+1} & \cdots & \vdots \\ \vdots & \vdots & \cdots & \vdots \\ h_{U-1} & h_{2U-1} & \cdots & h_{KU-1} \end{bmatrix} \begin{bmatrix} x_n \\ x_{n-1} \\ \vdots \\ x_{n-U} \end{bmatrix} = \begin{bmatrix} P_0 \\ P_1 \\ \vdots \\ P_{U-1} \end{bmatrix} \times \begin{bmatrix} x_n \\ x_{n-1} \\ \vdots \\ x_{n-U} \end{bmatrix} \tag{4}$$

In eqn. 4 the y_n represent the up-sampled and interpolated sequence, the h_n are the M-tap coefficients of the interpolation filter and the P_n are the K-tap polyphase filter sections. The function of the polyphase filter as a fractional delay element is to select one of the U values of the y_n for every x_n input, that is, there is no sample rate change overall. This is equivalent to filtering the input x_n with a changing polyphase filter section P_l dependent on the fractional delay l/U that is required. Such a switched-coefficient filter would then be time-variant.

Complete algorithm including bulk delay: Bulk delay can be included by simply extending the shift register containing the input x_n by $B - 1$ and offsetting the filtering operation by the bulk delay required, d, with $0 \leq d < B$.

The complete algorithm is as follows:

(i) input the required delay, τ_e

(ii) shift data, x_n, into $K + B - 1$ length register

(iii) reduce the input delay modulo B by putting

$$m = \begin{cases} \lfloor \tau_e U \rfloor / U \bmod B + B & \text{if } \tau_e < 0 \\ \lfloor \tau_e U \rfloor / U \bmod B & \text{if } \tau_e \geq 0 \end{cases} \tag{5}$$

(iv) fix bulk delay d as

$$d = B - 1 - \lfloor m \rfloor \tag{6}$$

(v) fix fractional delay u as

$$u = (m - \lfloor m \rfloor) \times U \tag{7}$$

(vi) filter the data and output the interpolated sample

$$y_{n-u} = \sum_{i=0}^{K} P_{u_i} x_{i+d} \tag{8}$$

Discrete-time S curves for NDA two-point tracker and DD four-point tracker: The S curve shows the expected output from the error-detection algorithm, $\varepsilon[e_t(n)]$, as a function of the delay.

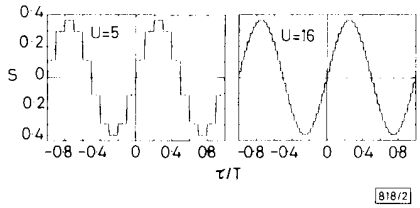

Fig. 2 *Discrete S curves for two-point Gardner algorithm produced with polyphase delay element with different values of upsample*

The performance of the algorithm introduced here is shown in the S curves in Fig. 2 for the two point NDA Gardner algorithm and in Fig. 3 for the four point DD algorithm. The input binary-antipodal data stream is filtered with a raised-cosine filter with rolloff factor $\beta = 0{\cdot}8$ and the curves are generated by averaging over 5000 symbols. A raised-cosine filter was used as an approximation to the ideal interpolation filter [5]. The results in Fig. 2 compare the performance of the discrete-time delay element with the continuous-time theory in Reference 2 where it is shown that the S curve is given by a sinusoid as

$$\varepsilon[e_t(n)] = -\frac{4}{T}\sin\left(\frac{2\pi\tau}{T}\right) \times \int_0^{1/T} G(f)G\left(\frac{1}{T} - f\right)\sin(\pi f T)\, df \tag{9}$$

In eqn. 9 T is the sample period and $G(f)$ is the frequency pulse corresponding to the PAM data stream. Note that the value of the integrand in eqn. 9 is in fact the gain of the S curve and is proportional to the excess bandwidth of $G(f)$.

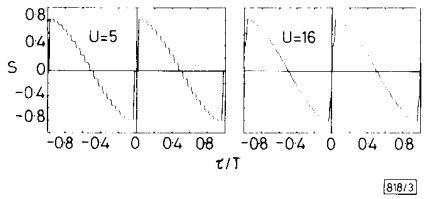

Fig. 3 *Discrete S curves for four point DD algorithm ($\alpha = 1{\cdot}0$) produced with polyphase delay element with different values of upsample*

Note that as the upsample factor is increased from $U = 5$ to $U = 16$ the shape of the S curve approaches that of the ideal.

Acknowledgments: The authors would like to thank the Defence Research Agency, Malvern, for their continued support for this research.

28th January 1993

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13 Gbit/s Si BIPOLAR PREAMPLIFIER FOR OPTICAL FRONT ENDS

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Indexing terms: Integrated circuits, Amplifiers

A preamplifier IC for a 10 Gbit/s optical fibre link was realised in a 0·8 μm silicon bipolar preproduction technology. Data rates up to 13 Gbit/s at high transimpedance (615 Ω) and low noise (10·5 pA/√(Hz) for 10 Gbit/s) were achieved. The frequency response can be individually optimised by adjusting a novel on-chip network via external potentiometers.

Introduction: In receivers for long-distance optical-fibre links a low-noise preamplifier is required which is directly driven by the photodiode. At high data rates this amplifier, which is usually of the transimpedance type, is one of the most critical circuits in the link because of the strong tradeoff between high bandwidth and high sensitivity (low noise). To the best of the authors' knowledge the highest data rate reported for silicon preamplifiers is 10 Gbit/s [1, 2]. The highest cutoff frequency of 15·5 GHz is reported in Reference 3 but without giving the maximum achievable data rate. In all these cases the cost of the high speed was the use of a low shunt feedback resistance (only 270 Ω in Reference 3), which degrades the noise behaviour (not given in References 1–3) and, moreover, causes a decrease in the transimpedance.

In this Letter a preamplifier for a 10 Gbit/s optical-fibre transmission system is developed. The circuit had to be designed in such a manner that, in contrast to Reference 1, no external (off-chip) equalising network is required. Moreover, the equivalent input noise current density should be low enough to allow the use of commercially available *pin* photodiodes at sufficient receiver sensitivity, and the transimpedance should be high enough to reduce the demands on the driven main amplifier, with respect to input sensitivity and voltage gain.

Circuit concept and design: Fig. 1 shows the circuit diagram of the preamplifier on the chip as well as the driving and loading circuitry for measuring the electrical characteristics. The photodiode (PD) is modelled by a simple network. The amplifier consists of a transimpedance stage with a comparatively high shunt feedback resistance $R_F = 615\,\Omega$, two emitter followers for impedance transformation and broadband level shifting, as well as an output transadmittance stage ($R_S = 20\,\Omega$) for driving matched 50 Ω transmission lines. The latter stage also allows the frequency response to be optimised by using peaking capacitors C1 and C2 as well as a special network (NW) for optimal adjustment of the frequency response (see below). The capacitors are realised by the emitter and collector junction capacitances of a transistor connected in parallel (emitter–collector short). C3 and C4 are external (off-chip) decoupling capacitors. An on-chip output resistor $R_Q = 100\,\Omega$ is provided to reduce double reflections and thus time jitter. Here, the low-frequency value of the total transimpedance Z_{TI} equals the feedback resistance R_F. The strong increase of the equivalent input noise current density with increasing frequency can be reduced by properly adjusting the input bond inductance L1 (~1·5–2 nH) to the capacitance C_{PD} of the photodiode (see Fig. 1).

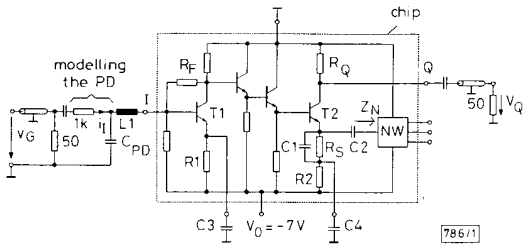

Fig. 1 *Circuit diagram of preamplifier chip and driving circuitry*
Resistances are given in Ω

The approach in Fig. 1 shows a negative shunt feedback R_F only over a single stage. The advantages compared to the feedback over several stages were discussed in Reference 4. One main advantage is that a flat frequency response of both the magnitude and the phase delay, required for optimum eye diagrams, can be easily adjusted by peaking. For this, besides the constant capacitor C1 shunting the feedback resistor R_S, a second capacitor C2 is provided which is connected to the output of the novel network NW in Fig. 2, consisting of two cascaded emitter followers. It can be shown that a large area of complex values for the output impedance Z_N can be covered by adjusting the collector currents of T3 and T4 (via the potentiometers P1 and P2). Moreover, C2 can be changed by varying the voltage across the corresponding *pn* junctions via P3. Thus the impedance of the series connection of C2 and Z_N can easily be adjusted with respect to the desired frequency response of the amplifier. The cutoff frequency of the amplifier reaches the lower limit if the influence of C2 is minimised by switching off the collector current of T3. Such a possibility of simply influencing the frequency response of the front end after chip fabrication and mounting is highly recommended especially in the early stages of system and technology development in order to be able to compensate for several uncertainties in this stage.

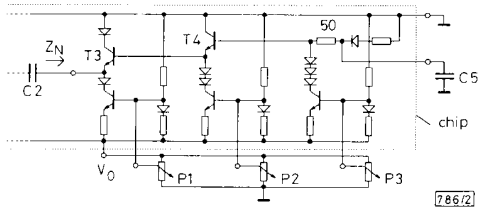

Fig. 2 *Network NW in Fig. 1 for optimising the frequency response of the preamplifier via external potentiometers*
C5 is a decoupling capacitor

The preamplifier was designed on the basis of a selfaligning double-polysilicon preproduction technology of Siemens characterised by a 0·8 μm lithography and a nominal transit frequency of 25 GHz ($V_{CE} = 1$ V). The technology has been described in Reference 5 and typical transistor parameters are given, for example, in Reference 6. According to the intended application in a digital system, the main aim was to achieve maximum data rate at sufficient input sensitivity rather than maximum cutoff frequency. At the desired data rate the cutoff frequency should be chosen to be as low as possible, by properly adjusting the network NW, in order to increase the input sensitivity (due to the reduction of the noise bandwidth).

Experimental results: The presented experimental results were achieved with the first technological run and without needing any redesign. For the direct measurement of the preamplifier, the chip was mounted unpackaged on a thin film ceramic substrate (16 × 13 mm²) using a conventional bonding technique. This test fixture contains all the external components