

A Broadband Wireless Packet Technique Based on Coding, Diversity, and Equalization

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ABSTRACT The choice of an air interface technique to enable broadband wireless communications has been the subject of extensive research. This article describes an air interface for 2 Mb/s wireless mobile packet data services. The key enabling technique is a reduced-complexity broadband equalizer which provides a delay spread tolerance of up to 50 μ s. The proposed air interface emphasizes high packet throughput, robust performance, low packet overhead, and low-cost low-power VLSI implementation.

The popularity of cordless and cellular phones today is an indication that there will be a mass market opportunity for wireless data terminals as well as broadband wireless services. There are two distinct, yet complementary, system approaches for addressing the demand for mobility: an enhanced cellular network with increased bit rate capabilities, and a noncentralized wireless local area network (LAN). The two system approaches are complementary because the wide-area cellular network permits high mobility and globalized communications through handoff and roaming, while wireless LANs can offer orders of magnitude higher data rates through coverage area restriction, which results in substantially reduced signal attenuation and multipath delay spread. Both system approaches have been the focus of extensive research and standards activities [1-3].

Major considerations for the choice of an air interface technique to enable wireless data include:

- **Flexible data rates:** In order to support bandwidth-on-demand services, the wireless link must offer a high peak data rate and a means for traffic multiplexing.
- **Low power consumption:** Power consumption is an issue because wireless terminals use battery power. In addition, broadband services will require increased power for both RF radiation (to overcome the increased thermal noise bandwidth) and signal processing. Advanced signal processing techniques will enable the receiver to operate at a low signal-to-noise ratio (SNR), thus reducing the RF power requirement. On the other hand, although advances in integrated circuits promise power reduction in future signal processing devices, this alone may not compensate for the ever more complex demand for broadband wireless receivers. It is important that the air interface technique emphasize reduced complexity.
- **High frequency reuse efficiency:** In a cellular system, high frequency reuse translates into low required bandwidth. This is important because, due to spectrum congestion, broadband services will face limits on the total amount of bandwidth available. High frequency reuse can be achieved with a number of cochannel interference management techniques [4], such as improved cellular engineering, power control, frequency hopping, and dynamic channel assignment. In addition, receiver techniques such as interference cancellation and smart antennas will enable the receiver to operate at a low required signal-to-interference ratio (SIR).

- **Low transmission overhead:** Transmission overhead includes guard bands, guard times, coding redundancy, and all the bandwidth (frequency/time/code) dedicated for

the purpose of receiver training and acquisition.

- **Robustness:** The air interface technique must be robust to different service environments, channel fading characteristics, and high mobility.

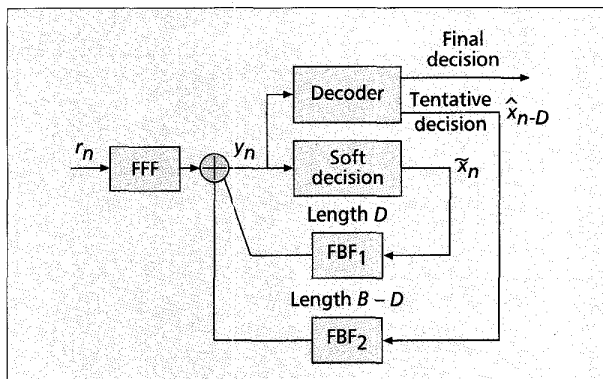
The word "broadband" has been used to imply a peak or aggregate data rate substantially higher than what today's digital wireless technologies can support. Based on a more specific (and perhaps less ambitious) interpretation, we consider a data rate on the order of 1 or 2 Mb/s for a wide-area cellular approach with a specified (e.g., in North America) maximum delay spread of 40 μ s, and 20 Mb/s for wireless LANs with a 10 times lower maximum delay spread. Possible air interface techniques for such applications include:

- Broadband code-division multiple access (CDMA) [2]
- Orthogonal frequency-division multiplexing (OFDM) [5]
- Equalized quaternary phase shift keying (QPSK) using a decision-feedback equalizer (DFE)

Each option has its own strengths and challenges. CDMA techniques use spread spectrum modulation, which inherently requires a significant bandwidth expansion for each "code." In order to support a high peak data rate within a limited bandwidth, a broadband CDMA approach must rely on multicode transmission and/or interference cancellation [2]. A CDMA system also requires fast and accurate feedback power control, which does not lend itself well to short packet data transmission.

OFDM can be viewed as a multicarrier modulation approach. The total signal bandwidth is divided into many narrowband subchannels to be transmitted and received in parallel. This obviates the need for equalization. OFDM also permits the use of "tone" sensing techniques to facilitate dynamic channel assignment [6]. A well-known disadvantage of OFDM is that the signal has a large peak-to-average power ratio. Thus, it requires the use of highly linear transmit amplifiers, which are not power-efficient. OFDM is also more sensitive to frequency offset than a single-carrier approach.

The broadband wireless technique described in this article is based on the equalized QPSK approach. A widely assumed limitation for this approach is that the required length of the equalizer grows linearly with the bit rate, leading to fundamental tracking problems and excessive complexity. A DFE is also notorious for error propagation. These and other limitations have been addressed in a series of research efforts on reduced-complexity broadband equalization and a joint coding and DFE scheme for remedying the error propagation prob-



■ **Figure 1.** A joint coding and DFE scheme, where FFF denotes feedforward filter and FBF denotes feedback filter. B is the total number of feedback filter taps.

lem [7–10]. This article summarizes the outcome of these efforts and describes an overall air interface proposal for 2 Mb/s wireless mobile packet data based on this equalizer approach. Although emphasis is placed on the wide-area cellular approach, many of the proposed concepts are applicable to other wireless scenarios, such as high-speed LANs.

We begin by giving a top-down description of the proposed air interface. Performance results are then presented, followed by a summary of an equalizer prototyping effort. The latter shows that the proposed equalizer concept is reducible to practice in a cost-effective way (in terms of power, size, and cost).

PROPOSED AIR INTERFACE BASED ON EQUALIZED QPSK

SUMMARY OF TECHNIQUES

The key air interface techniques include:

- QPSK modulation (symbol period = 1 μ s)
- Rate-1/2 convolutional coding without interleaving
- Two-branch receiver diversity
- Two-branch transmitter diversity with one-symbol delay between antennas
- Reduced-complexity DFE with a delay spread tolerance up to about 50 μ s

Note that interleaving is not used because we assume a system which transmits short data packets.

JOINT CODING AND EQUALIZATION

Rate-1/2 convolutional coding with a constraint length of 6 was chosen (a longer constraint length was found to provide little additional coding gain while requiring higher complexity). The major challenge associated with the use of coding and DFE is the problem of error propagation. Most coding techniques are designed to correct random errors. A DFE, on the other hand, produces errors that are bursty in nature, due to the fact that the DFE relies on delay-free hard decisions (before decoding) to cancel intersymbol interference (ISI) in subsequent data symbols. Decision errors tend to trigger strings of improper ISI cancellation. The resulting error propagation severely limits the achievable coding gain of any coding technique. A number of schemes have been proposed in the past to remedy the error propagation problem (Tomlinson precoding, use of a noise-predictive feedback filter structure with interleaving, etc.). However, these solutions are either impractical or inadequate for the broadband wireless scenario under consideration.

The scheme we propose uses a combination of soft decisions and delayed tentative decisions from the error correction decoder (i.e., a Viterbi decoder) to cancel ISI in the feedback path of the DFE [9]. As shown in Fig. 1, the feed-

back filter of the DFE is divided into two parts, FBF₁ and FBF₂. Soft decisions are used in FBF₁ to suppress ISI due to multipath with short delays; and tentative hard decisions, with delay D typically equal to the constraint length of the convolutional code, are used in FBF₂ to cancel ISI due to multipath with large delays.

The use of soft decisions to combat error propagation is not new. However, previously proposed techniques are based on maximum *a posteriori* probability (MAP) algorithms [11]. While optimum, these MAP approaches require more computations than the Viterbi decoder itself. In contrast, our soft decision method, derived by approximating a MAP approach, requires only the simple operation of passing the real and imaginary parts of the DFE output through a hyperbolic tangent function

$$\tilde{x}_n = \frac{1}{\sqrt{2}} \left(\tanh(\sqrt{2} \operatorname{Re}(y_n)) + j \tanh(\sqrt{2} \operatorname{Im}(y_n)) \right), \quad (1)$$

where the ideal QPSK symbol value is

$$x_n = \pm \frac{1}{\sqrt{2}} \pm \frac{j}{\sqrt{2}},$$

and subscript n indicates the n th data symbol. Results in [9] showed that this simple method performs almost as well as the optimum soft feedback approach based on MAP. When further combined with tentative decisions from the Viterbi decoder, the proposed soft/delayed feedback DFE (S/D-DFE) can practically eliminate the problem of error propagation in broadband wireless channels (see an example of performance results in the next section).

DIVERSITY

The proposed air interface includes the use of diversity at both the transmitter and the receiver. Transmitter diversity is used to combat flat fading. Since flat fading is often a performance-limiting case in equalized wireless links, we propose the use of two transmitting antennas with one-symbol delay between them to deliberately create a controlled multipath effect; that is, a flat fading signal will be received as if the channel were a two-path fading channel.

Receiver diversity provides a few well-known benefits, such as lower required SIR and SNR, robustness to high mobility, and possible cochannel interference suppression. The proposed air interface uses a two-branch diversity receiver with a separate feedforward filter (with eight taps) on each branch, and a common feedback filter (with 50 taps) placed after combining. All the filters are jointly optimized using a least mean square (LMS) algorithm. Therefore, the diversity combining scheme is equivalent to minimum mean square error (MMSE) combining in the sense that it provides interference suppression (this capability is not exploited in this article because we assume cochannel interference to be Gaussian).

REDUCED-COMPLEXITY EQUALIZATION

The key enabling techniques to low-complexity DFE are [7, 8]:

- Modified DFE structure permitting a training-free and multiply-free feedback filter
- Unbalanced feedforward and feedback spans, that is, a significantly reduced number of feedforward taps
- Channel-estimation-based timing recovery, optimizing the decision delay relative to the channel impulse response
- Selectable feedforward tap spacings to increase the feedforward span without increasing the number of taps

Figure 2 shows an example of the modified DFE structure [7] which we use for equalizer training. Unlike a conventional DFE structure where the feedback filter is placed after the feedforward filter, the feedback filter in the modified structure is "interlaced" with the feedforward filter. Namely, past-symbol

ISI is precanceled from each feedforward tap before multiplying with a feedforward coefficient a_i , where $i = 0, 1, \dots, F - 1$. This ISI precancellation is done by convolving the channel estimates $\{\hat{h}_k\}$, obtained prior to equalizer training, with detected QPSK symbols (known training symbols in our case). Since the QPSK symbols are representable by $\pm 1 \pm j$, all the computations required can be implemented using adders (i.e., the *multiply-free* feature is actually due to QPSK modulation and hard decision rather than to the modified structure). Accordingly, we only need to train the feedforward filter, which in our case has only eight taps, so fast training can be achieved even with a simple LMS algorithm.

With the feedback filter training-free and multiply-free, we let the feedback filter be as long as necessary (i.e., 50 taps). The number of feedforward taps must be minimized, since it now dictates the complexity and training requirements. Three factors contribute to the reduced number of feedforward taps chosen.

First, we recognize that the length of the feedforward filter need not grow linearly with the channel dispersion. In an approximate sense, when the length of the feedback filter is sufficient, the feedforward filter is used to "capture" multipath energy, similar to what a RAKE combiner does in a CDMA receiver. As delay spread increases, a fixed-length filter may not be able to span the entire impulse response, but the receiver can take advantage of the increased number of resolved paths to achieve better multipath diversity. As a result, we usually find a DFE with a fixed-length feedforward filter to give relatively stable performance over a broad range of delay spread [7].

Two other factors contributing to a low required number of feedforward taps are the timing recovery technique and the tap-selectable structure we have proposed. The timing recovery technique [7] performs burst synchronization, which can also be viewed as optimizing the delay j (Fig. 2) of the first feedforward tap for a conventional contiguous-tap DFE. Such optimization has been shown to critically affect the performance of

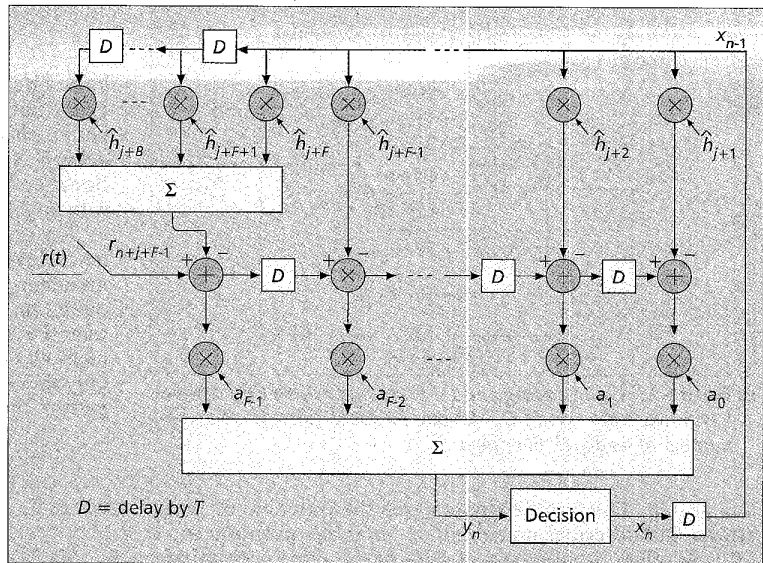


Figure 2. A modified DFE with F feedforward taps and B feedback taps.

a finite-length DFE (e.g., [7]). We have also proposed a technique to optimize the spacings between different feedforward taps so that, when the channel consists of sparsely distributed multipath, the taps can also be sparsely assigned to wherever energy is concentrated (similar to an *adaptive RAKE* receiver) [8]. Both timing recovery and tap selection are performed prior to equalizer training and are based on the use of channel estimates. In our proposal we use a combination of contiguous and sparse tap assignments, that is, out of the eight taps, the first four are contiguous, and the last four variably assigned using an Uncorrelated ISI (UISI) algorithm [8].

OVERALL RECEIVER STRUCTURE

Figure 3 shows the overall baseband receiver structure of our proposal. Part of this receiver has been implemented in a prototyping effort to be described later. The receiver consists of three pipelined units to allow continuous reception of consecutive data packets. The received signal is sampled at four times the symbol rate. After analog-to-digital (A/D) conversion the received signal samples are stored in a buffer memory while a number of estimations are executed, including channel estimation, symbol and burst timing estimation, and the estimation of optimum feedforward tap spacings.

Channel estimation is performed on the received sync word of 126 symbols, which we referred to as the training overhead. The sync word is transmitted in the beginning of each data packet. It includes two periods of a pseudo-noise (PN) sequence of length 63. Only the second period of the PN sequence is used for channel estimation and training, since the first period of the PN sequence can be corrupted by the dispersion of a previous data packet and/or by unsettled adaptive gain control (AGC) acquisition.

The channel estimator is implemented using a hardware cyclic correlator [10] of length 63. The remaining estimations are done using a digital signal processor (DSP). This DSP has a low

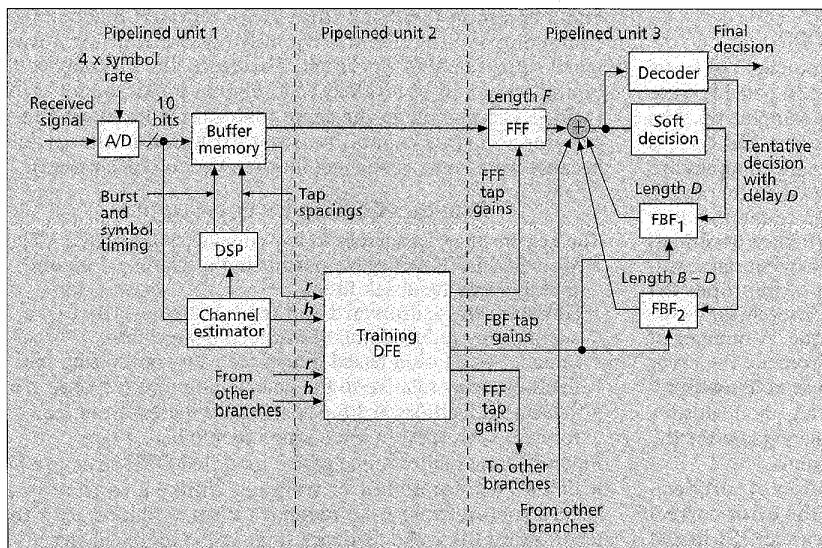
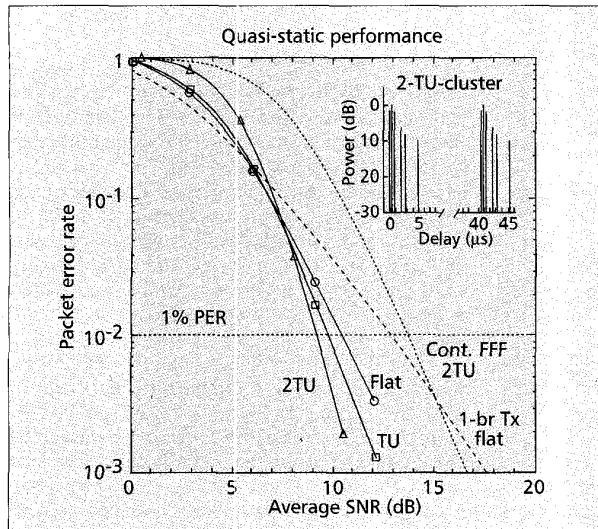
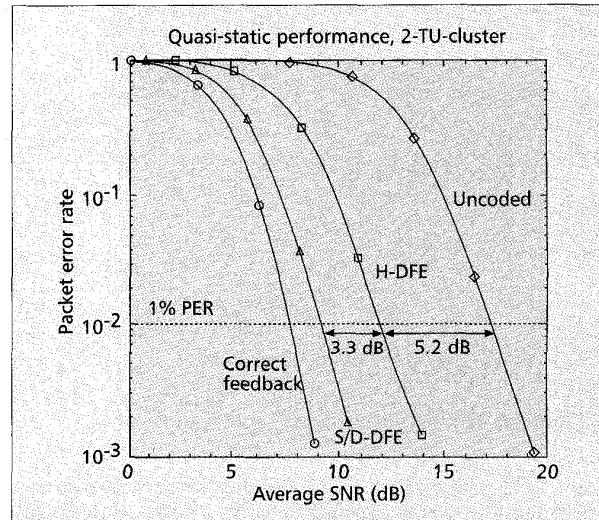


Figure 3. Overall receiver structure.



■ Figure 4. Performance of the proposed air interface technique.



■ Figure 5. Coding gain improvement of the proposed joint coding and DFE scheme.

speed requirement — say, less than 10 million instructions per second (MIPS) — because the estimations are allowed to use up the remaining time of the entire packet. The estimated timings and tap spacings are used to gate the received signal samples from the buffer memory. These data samples (\mathbf{r}), along with the channel estimates (\mathbf{h}), are passed on to the second pipelined unit, the modified DFE.

The modified DFE performs training of the feedforward filters based on the same sync word (only the last 63 symbols) used in channel estimation. The sync word is repeated three times to allow initial convergence. Channel estimates are used to pre-cancel past-symbol ISI, as mentioned earlier. After training, the feedforward filter tap gains are convolved with the channel estimates to obtain the actual feedback filter tap gains. All the filter tap gains are then forwarded to the data detection DFE.

The third pipelined unit is the data detection DFE. This is implemented based on the joint coding and DFE scheme already shown in Fig. 1. The tentative delay D is set to 5 in our case. During data detection, all the taps are adapted based on the tentative decisions. The third pipelined unit also allows for a fine-tuning process before actual data detection. In this process, all the equalizer taps are simultaneously readjusted using the sync word. The purpose of fine tuning is to minimize the effect of noisy channel estimates on the quality of initial training done by the modified DFE [7].

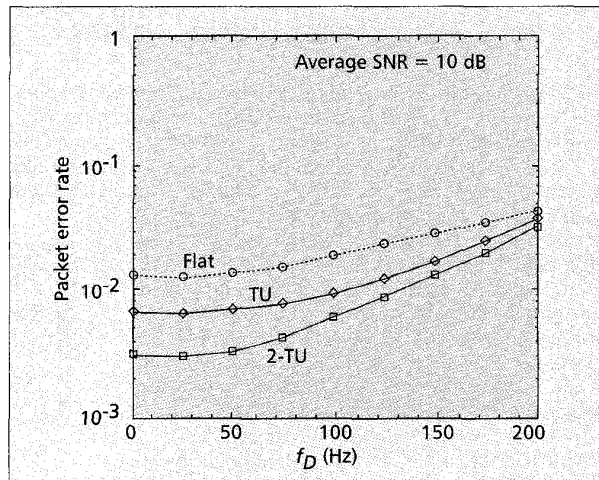
PERFORMANCE

Figures 4 to 6 show examples of the performance of the proposed air interface. The performance is given in terms of the average packet error rate over Rayleigh fading, where each packet contains a payload of 800 symbols and a training overhead of 126 symbols. All these results are obtained from fixed-point simulations that match a specific prototype design, to be described in the next section. They include implementation losses, such as the effects of finite arithmetic, imperfect timing recovery and equalizer training, and noisy channel estimates.

Figure 4 shows results for different delay profiles:

- Flat fading
- The Global System for Mobile Communications' (GSM's) typical urban (TU) profile
- A two-TU-cluster (2TU) profile

The 2TU profile, shown in the inset of Fig. 4, consists of two TU profiles separated from each other by $40.5 \mu\text{s}$. This profile is used to represent an extreme case for highly dispersive envi-

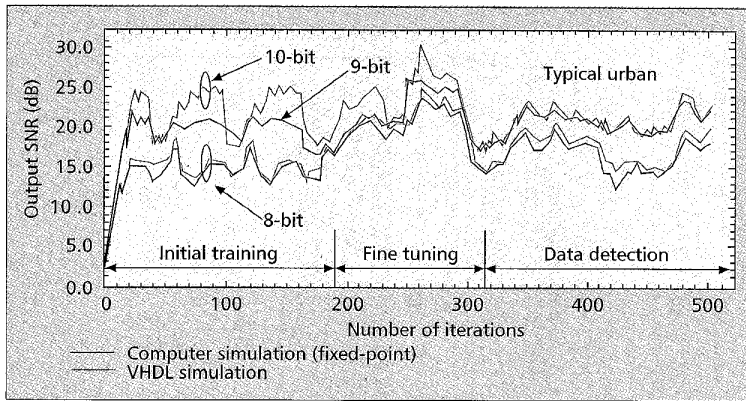


■ Figure 6. Fast fading performance.

ronments. In all the profiles, we assume that each path is independently Rayleigh fading, and the fadings are uncorrelated on all the links between different transmit and receive antennas. The solid lines in Fig. 4 are performance curves for the proposed receiver. This receiver can achieve a 1 percent packet error rate (PER) at an average SNR around 10 dB for all profiles. The dashed lines are performance curves for the receiver without certain elements; these are plotted to show that transmitter diversity and adaptive tap assignment are both needed to protect against pathological profiles. With only one transmitter antenna, the receiver would require 3 dB higher SNR to achieve 1 percent PER in flat fading. Without the tap selectable structure, the performance for the 2TU profile would be degraded by as much as 5 dB.

Figure 5 demonstrates how well the proposed joint coding and DFE scheme performs under a highly dispersive channel model. Compared to a conventional hard-decision DFE (H-DFE), the proposed S/D-DFE gives an additional coding gain of 3.3 dB; and it performs to within 1.5 dB of ideal performance without error propagation (the curve labeled "Correct feedback").

Results in Figs. 4 and 5 are based on the assumption of quasi-static fading (i.e., the channel is stationary over the dura-



■ Figure 7. The effect of word length on implementation.

tion of each data packet). Figure 6 shows the performance as a function of the Doppler frequency f_D , for a given average SNR of 10 dB (time-correlated Rayleigh fading was simulated using the Jakes' model [12]). The proposed receiver is found to be quite robust to time-varying channels.

THE EQUALIZER PROTOTYPING EFFORT

An important attribute of the proposed equalizer approach is that the DFE has a standard digital filter structure, thus lending itself well to dedicated hardware realization. If implemented using general-purpose DSPs, the proposed receiver would require a processing speed on the order of 1000 MIPS, and would have a power consumption on the order of several watts (assuming the most advanced DSP/device technology to date). However, the use of MIPS to measure complexity and power consumption no longer applies for implementation using dedicated hardware. For example, we show later that the estimated power consumption of the proposed DFE is even less than 1 W when implemented with dedicated hardware.

We have implemented the proposed DFE in VHSIC Hardware Description Language (VHDL). VHDL [13] is a powerful tool for designing and testing prototype hardware. It can represent a design model at different levels of abstraction, from a register transfer level (RTL) to behavioral modeling. It also supports multiple simulation objectives, including functional simulation, timing simulation, and gate synthesis targeting specific device options.

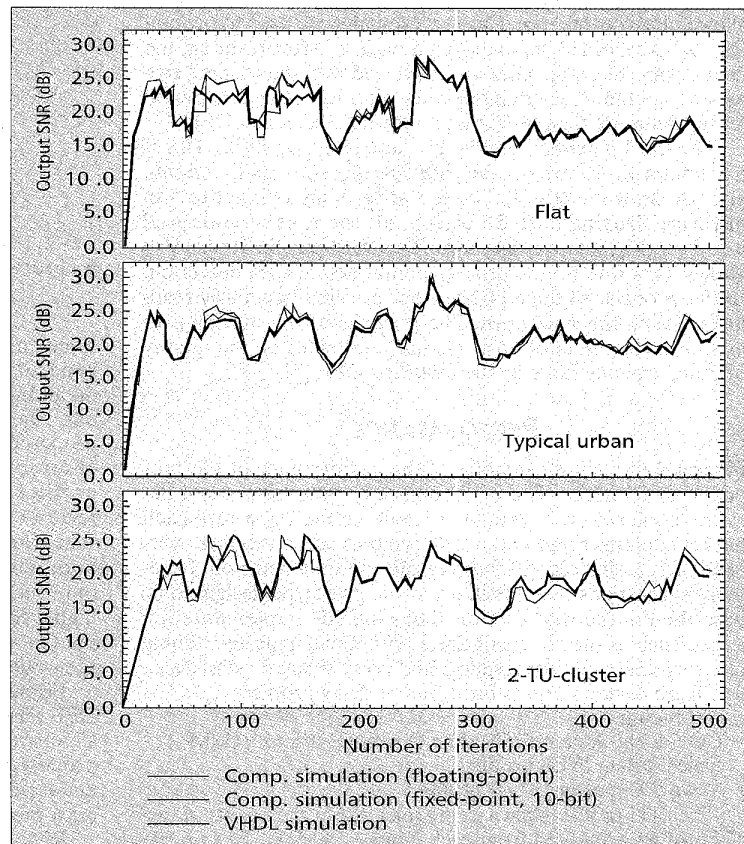
Details regarding the implementation study are described in [10]. The design follows the pipelined architecture in Fig. 3. Receiver hardware represented in RTL includes the channel estimator, modified DFE, data detection DFE (without error correction), and control of all receiver operations. Associated hardware, such as the buffer memory and DSP, are described with higher-level representations. In the design verification, a minimum configuration is used which includes only one receiving branch instead of two, and five contiguous feedforward taps instead of eight contiguous/selectable feedforward taps. This minimum configuration, however, contains all the processing units that can be replicated to implement the complete receiver with diversity.

Figures 7 and 8 illustrate the results of the

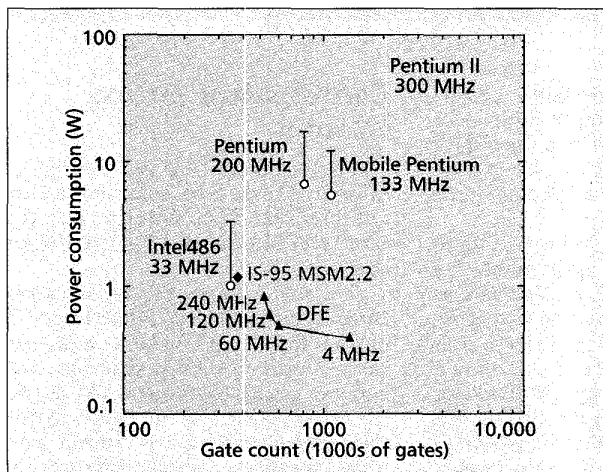
design verification. Each plot represents the *learning curve* of the DFE, where the output SNR is computed by averaging the squared error over 16 symbol periods, and the channel is assumed to be stationary (i.e., a snapshot of the Rayleigh fading process). As depicted in Fig. 7, the learning curve includes three different phases: initial training (the first 189 iterations), fine tuning (126 iterations, i.e., the sync word is repeated twice), and data detection (shown only for 200 symbols).

Figure 7 shows the effect of *word length*, which refers to the fixed-point resolution of both the input signal and the DFE tap coefficients. The red curves represent the results of the VHDL design (a 9-bit version was not implemented), while the black are results generated by fixed-point computer simulation; the two sets of results agree with each other very well. Based on these results, we chose to implement the 10-bit version, and we also incorporated this word length into the radio link simulator to obtain performance results in Figs. 4 to 6. Figure 8 shows results for different delay profiles. Also added in this figure, in blue, are results obtained from floating-point computer simulation. Due to the strong agreement between the results of VHDL design and those of both fixed-point and floating-point computer simulations, we are extremely confident in both the accuracy of the prototype design and the feasibility of the proposed equalizer concept.

Through VHDL synthesis we can obtain an accurate esti-



■ Figure 8. Design verification assuming 10-bit resolution.



■ Figure 9. Estimates of gate count and power consumption.

mate of the design complexity. Figure 9 shows the estimated gate count and power consumption of the proposed DFE (based on the complete receiver structure with diversity). For reference, we provide available data for a family of Intel processors and Qualcomm's IS-95 Mobile Station Modem (MSM) chip. Note that the power consumption estimates for the DFE are based on 0.25 μm technology, whereas the others are based on 0.35 μm and higher.

Our implementation study provides different trade-offs between gate count and power consumption. This is due to the different possible design options. For example, in order to implement a 50-tap filter, one can represent all 50 taps by exclusive logic in order to minimize the required clock rate and power consumption. Or one can use shared logic running at a higher clock rate (i.e., resource sharing) to provide the same result. The result for a clock rate of 4 MHz in Fig. 9 represents a design using exclusive logic, while results for higher clock rates use resource sharing to minimize the gate count. In terms of power consumption, all design options provide promising numbers for wireless applications (i.e., less than 1 W). Thus, if we select the 120 MHz design as an optimum option, the gate count is 600,000 kgates, or about 1.6 times that of the Intel 486. Since an Intel 486 processor using 0.6 μm technology has physical dimensions comparable to a U.S. quarter, the DFE using 0.25 μm technology could conceivably be as small as a U.S. dime!

CONCLUSION

Equalization techniques used in current digital cellular standards may not be scalable to much higher data rates, due to the growing complexity and fundamental tracking problems. However, our research efforts have shown that an equalizer approach is still a viable option for future broadband wireless transmission. In fact, the proposed equalizer technique is readily realizable at possibly low cost and low power with current VLSI technology, and can provide nearly transparent performance, in terms of the required training overhead percentage, coded link performance, and robustness to high mobility, compared to narrowband wireless systems without equalization. Co-channel interference suppression is also possible, since the proposed receiver with diversity can automatically suppress dominant interferers whenever there is a sufficient degree of freedom.

The ability to suppress dispersive interference can be

enhanced by modifying the feedforward tap assignment algorithm to take the interference characteristics into account; research is ongoing in this area. Another area of research is in enhancing the spectrum efficiency of the system through appropriate use of advanced channel access protocols [4]. Providing a path to such technology evolution is crucial to the progress of broadband wireless research.

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BIOGRAPHIES

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